

CLAIMS

What is claimed is:

1 1. A method of forming an interconnection, comprising
2 introducing a barrier material in a via of a dielectric to
3 a circuit device on a substrate in such a manner to deposit the
4 barrier material on the circuit device;

5 introducing a seed material into said via in a manner that
6 leaves the barrier material overlying the circuit device
7 substantially exposed;

8 substantially removing the barrier material overlying the
9 circuit device; and

10 introducing a conductive material in the via to form the
11 interconnection.

1 2. The method of claim 1, wherein the step of introducing
2 a seed material comprises sputter depositing the seed material
3 into the via.

1 3. The method of claim 1, wherein the barrier material
2 comprises etch characteristics such that the barrier material
3 may be selectively etched in the presence of the seed material.

1 4. The method of claim 1, wherein the circuit device is
2 an interconnection line.

1 5. The method of claim 1, wherein the step of introducing
2 the conductive material comprises electroplating.

1 6. A method of forming an interconnection on a substrate,
2 comprising:

3 providing a substrate having a circuit device, a dielectric
4 material overlying the circuit device having a via through the
5 dielectric to the circuit device;

6 depositing a barrier material in the via to substantially
7 cover the side walls of the via and the circuit device;

8 introducing a seed material into said via in a manner that
9 leaves the barrier material overlying the circuit device
10 substantially exposed;

11 substantially removing the barrier material overlying the
12 circuit device; and

13 introducing a conductive material in the via to form the
14 interconnection.

1 7. The method of claim 6, wherein the step of introducing
2 a seed material comprises sputter depositing the seed material.

1 8. The method of claim 7, wherein the step of introducing
2 a seed material comprises introducing the seed material over a
3 portion of a top surface of the dielectric material and an
4 amount of seed material over the barrier material overlying the

5 circuit device is about five percent or less of the amount
6 overlying the top surface of the dielectric.

1 9. The method of claim 6, wherein the barrier material
2 comprises etch characteristics such that the barrier material
3 may be selectively etched in the presence of the seed material.

1 10. The method of claim 6, wherein the circuit device is
2 an interconnection line.

1 11. The method of claim 6, wherein the step of introducing
2 a conductive material comprises electroplating.

1 12. An integrated circuit comprising:
2 a substrate having a circuit device;
3 a dielectric material overlying the circuit device with a
4 via formed in the dielectric material to the circuit device;
5 a barrier material substantially lining ^{at least one wall} ~~a wall or walls~~ of
6 the via;
7 a seed layer overlying the barrier material and substantial
8 lining the ~~wall or walls~~ of the via; and
9 a conductive material directly contacting the circuit
10 device.

1 13. The integrated circuit of claim 10, wherein the
2 circuit device is an interconnection line

B' which
1 14. The integrated circuit of claim 10, wherein the
2 conductive material is copper.

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